CLAIM AMENDMENTS

1. (original) A digital signal processing based serializer/de-serializer, comprising:

a receiver that includes an analog to digital converter and a digital signal processor, the digital signal processor is operably coupled to an output of the analog to digital converter;

wherein the analog to digital converter samples modulated serial data to generate digital samples of the modulated serial data; and

the digital signal processor adaptively determines compensation operations to be performed by the receiver on the digital samples of the modulated serial data so that the digital samples of the modulated serial data may be properly characterized to extract digital data contained therein.

2. (original) The digital signal processing based serializer/de-serializer of claim 1, wherein the digital signal processing based serializer/de-serializer interfaces two devices communicatively coupled via at least one of a twisted pair cable, a coaxial cable, and a twin-ax cable.

3. (original) The digital signal processing based serializer/de-serializer of claim 1, wherein the digital signal processing based serializer/de-serializer interfaces a first printed circuit board to a second printed circuit board.

4. (original) The digital signal processing based serializer/de-serializer of claim 1, wherein the digital signal processing based serializer/de-serializer interfaces a first integrated circuit to a second integrated circuit.

5. '(original) The digital signal processing based serializer/de-serializer of claim 4, wherein the plurality of integrated circuits are situated on a printed circuit board.

6. (original) The digital signal processing based serializer/de-serializer of claim 1, wherein at least one of the analog serial data and the digital data comprises fixed pattern noise.

7. (original) The digital signal processing based serializer/de-serializer of claim 6, wherein the digital signal processor determines compensation to be performed to substantially eliminate the fixed pattern noise.

8. (original) The digital signal processing based serializer/de-serializer of claim 6, wherein the fixed pattern noise is introduced during the digital sampling of the analog serial data by the analog to digital converter to generate the digital data.

9. (original) The digital signal processing based serializer/de-serializer of claim 1, wherein the digital signal processor determines a compensation operation to be performed on the analog serial data.

10. (original) The digital signal processing based serializer/de-serializer of claim 9, further comprising a programmable gain amplifier, communicatively coupled to the analog to digital converter; and

wherein the compensation operation comprises adjusting the gain of the programmable gain amplifier.

11. (original) The digital signal processing based serializer/de-serializer of claim 10, further comprising an automatic gain control circuitry; and

wherein the automatic gain control circuitry adjusts the gain of the programmable gain amplifier.

12. (original) The digital signal processing based serializer/de-serializer of claim 1, wherein the digital signal processor determines a compensation operation to be performed on the digital data.

13. (original) The digital signal processing based serializer/de-serializer of claim 1, wherein the digital signal processing based serializer/de-serializer is implemented in a data communications application.

14. (original) The digital signal processing based serializer/de-serializer of claim 1, further comprising a memory that comprises a plurality of compensation options;

wherein the digital signal processor selects at least one compensation option from the plurality of compensation options to ensure the proper characteristic of the digital data.

15. (original) The digital signal processing based serializer/de-serializer of claim 1, wherein the proper characteristic of the digital data comprises at least one of a gain, a phase, and an offset.

16. (original) The digital signal processing based serializer/de-serializer of claim 1, further comprising a transmitter and an interconnection; and

wherein the interconnection communicatively couples the transmitter and the receiver;

the transmitter transmits the serial data to the receiver via the interconnection;

the interconnection comprises a response that introduces an error into the serial data;

the digital signal processor determines the error introduced into the serial data by the response of the interconnection.

17. (original) The digital signal processing based serializer/de-serializer of claim 1, wherein the proper characteristic of the digital data comprises at least one of a gain, a phase, and an offset; and

the digital signal processor determines at least one of an error in gain, an error in phase, and an error in offset that is introduced during the digital sampling of the incoming, serial data signal by the analog to digital converter.

18. (original) The digital signal processing based serializer/de-serializer of claim 1, wherein the compensation determined by the digital signal processor comprises a compensation operation that comprises adjusting an operational parameter of the analog to digital converter.

19. (original) The digital signal processing based serializer/de-serializer of claim 1, further comprising an analog circuitry located before and communicatively coupled to the analog to digital converter; and

wherein the compensation determined by the digital signal processor comprises a compensation operation that comprises adjusting an operational parameter of the analog circuitry.

20. (original) The digital signal processing based serializer/de-serializer of claim 1, wherein the analog to digital converter comprises a plurality of analog to digital converters; and

each analog to digital converter within the plurality of analog to digital converters performs digital sampling of the incoming, serial data signal.

21. (original) The digital signal processing based serializer/de-serializer of claim 20, each analog to digital converter within the plurality of analog to digital converters performs digital sampling of a clock cycle of the analog serial data at a different time.

22. (original) The digital signal processing based serializer/de-serializer of claim 21, wherein the compensation determined by the digital signal processor comprises a compensation operation that comprises adjusting a first operational parameter of a first analog to digital converter within the plurality of analog to digital converters and a second operational parameter of a second analog to digital converter within the plurality of analog to digital converters.

23. (original) The digital signal processing based serializer/de-serializer of claim 22, wherein the first operational parameter and the second operational parameter comprise a common operational parameter.

24. (original) The digital signal processing based serializer/de-serializer of claim 22, wherein at least one of the first operational parameter and the second operational parameter comprises at least one of a gain, a phase, and an offset.

25. (original) The digital signal processing based serializer/de-serializer of claim 1, wherein the analog to digital converter comprises a plurality of analog to digital converters;

the analog serial data is partitioned into a plurality of channels; and

each channel of the plurality of channels communicatively couples to one analog to analog to digital converter within the plurality of analog to digital converters.

26. (original) The digital signal processing based serializer/de-serializer of claim 25, further comprising a plurality of programmable gain amplifiers;

the analog serial data is simultaneously fed to each programmable gain amplifier within the plurality of programmable gain amplifiers;

the outputs of the plurality of programmable gain amplifiers form the plurality of channels.

27. (original) The digital signal processing based serializer/de-serializer of claim 1, wherein the analog to digital converter comprises a plurality of analog to digital converters;

the analog serial data is simultaneously fed to each analog to digital converter within the plurality of analog to digital converters.

28. (original) The digital signal processing based serializer/de-serializer of claim 1, further comprising a precursor filter and an equalizer;

wherein the precursor filter is communicatively coupled to the analog to digital converter; and

the equalizer is communicatively coupled to the analog to digital converter.

29. (original) The digital signal processing based serializer/de-serializer of claim 28, wherein the equalizer comprises at least one of a feed forward equalizer, a feedback equalizer, and a decision feedback equalizer.

30. (original) The digital signal processing based serializer/de-serializer of claim 1, further comprising a decoder that is operable to decode the digital samples of the modulated serial data.

31. (original) The digital signal processing based serializer/de-serializer of claim 30, wherein the decoder comprises at least one of a Viterbi decoder, a convolutional decoder, a block code decoder, and a trellis decoder.

32. (original) The digital signal processing based serializer/de-serializer of claim 31, wherein the Viterbi decoder decodes inter-symbol interference within the modulated serial data.

33. (original) The digital signal processing based serializer/de-serializer of claim 31, wherein the Viterbi decoder comprises a partial response maximum likelihood decoder.

34. (original) The digital signal processing based serializer/de-serializer of claim 1, wherein the digital signal processing based serializer/de-serializer is operable to perform data communications at a speed higher than one Giga-bit per second.

35. (original) The digital signal processing based serializer/de-serializer of claim 1, wherein the digital signal processing based serializer/de-serializer employs parallel processing compensation techniques.

36. (original) The digital signal processing based serializer/de-serializer of claim 1, further comprising at least one additional digital signal processor that operates cooperatively with the digital signal processor.

37. (original) The digital signal processing based serializer/de-serializer of claim 1, wherein the digital signal processor is operable to perform digital signal processing on the digital data to ensure the proper characteristic of the digital data.

38. (original) The digital signal processing based serializer/de-serializer of claim 1, further comprising a crosstalk canceller communicatively coupled to the analog to digital converter; and

wherein the crosstalk canceller is operable to substantially eliminate at least one of near-end crosstalk and far-end crosstalk within the modulated serial data.

39. (original) The digital signal processing based serializer/de-serializer of claim 1, wherein the receiver further comprises an analog front-end that comprises a plurality of interleaves; and

the digital signal processor performs adaptive compensation to overcome impairment generated by non-uniformity among the plurality of interleaves.

40. (original) The digital signal processing based serializer/de-serializer of claim 39, wherein the analog front-end comprises a plurality of programmable gain amplifiers; and

the digital signal processor performs adaptive compensation to overcome impairment generated by non-uniformity among the programmable gain amplifiers.

41. (original) The digital signal processing based serializer/de-serializer of claim 39, wherein the analog front-end comprises a plurality of analog to digital converters; and

the digital signal processor performs adaptive compensation to overcome impairment generated by non-uniformity among the plurality of analog to digital converters.

42. (original) A transceiver, comprising:

a receiver comprising a plurality of analog to digital converters and a digital signal processor; and

wherein each analog to digital converter within the plurality of analog to digital converters digitally samples analog serial signal to generate digital data arranged across a plurality of channels, each channel of the plurality of channels extends from one analog to digital converter within the plurality of analog to digital converters; and

the digital signal processor adaptively determines a parallel based compensation and a parallel based operation to be performed to ensure a proper characteristic of the digital data.

43. (original) The transceiver of claim 42, wherein the parallel based operation comprises adjusting an operational parameter of at least one analog to digital converter within the plurality of analog to digital converters.

44. (original) The transceiver of claim 43, wherein operational parameter comprises at least one of a gain, an offset, and a phase.

45. (original) The transceiver of claim 43, wherein the adjusting of the operational parameter comprises employing timing recovery.

46. (original) The transceiver of claim 42, wherein proper characteristic of the digital data comprises at least one of a gain, a phase, and an offset.

47. (original) The transceiver of claim 42, wherein the digital sampling of the analog serial signal introduces an error into the digital data.

48. (original) The transceiver of claim 47, wherein the error comprises at least one of an error of gain, an error of phase, and an error of offset.

49. (original) The transceiver of claim 47, wherein the error comprises fixed pattern noise.

50. (original) The transceiver of claim 42, wherein the transceiver receives the analog serial signal via an interconnection; and

wherein the interconnection introduces an error into the analog serial signal.

51. (original) The transceiver of claim 50, wherein the error comprises at least one of an error of inter-symbol interference, attenuation, crosstalk, and noise.

52. (original) The transceiver of claim 42, wherein the analog serial signal is simultaneously fed to each analog to digital converter within the plurality of analog to digital converters.

53. (original) The transceiver of claim 52, wherein the digital signal processor provides parallel based control individually to each analog to digital converter within the plurality of analog to digital converters.

54. (original) The transceiver of claim 52, wherein the digital signal processor simultaneously provides a single control to each analog to digital converter within the plurality of analog to digital converters.

55. (original) The transceiver of claim 42, wherein the analog serial signal is partitioned into a plurality of channels before being fed to the plurality of analog to digital converters.

56. (original) The transceiver of claim 42, further comprising a plurality of programmable gain amplifiers;

wherein the analog serial signal is simultaneously fed to each programmable gain amplifier within the plurality of programmable gain amplifiers; and

each programmable gain amplifier within the plurality of programmable gain amplifiers communicatively couples to one analog to digital converter within the plurality of analog to digital converters.

57. (original) The transceiver of claim 56, wherein the gain of at least one programmable gain amplifier within the plurality of programmable gain amplifiers is adjusted using automatic gain control.

58. (original) The transceiver of claim 42, further comprising an equalizer.

59. (original) The transceiver of claim 58, wherein the equalizer comprises at least one of a feed forward equalizer, a feedback equalizer, and a decision feedback equalizer.

60. (original) The transceiver of claim 42, further comprising a decoder.

61. (original) The transceiver of claim 60, wherein the decoder comprises at least one of a Viterbi decoder, a convolutional decoder, a block code decoder, and a trellis decoder.

62. (original) The transceiver of claim 42, wherein the transceiver is operable to perform data communications at a speed higher than one Giga-bit per second.

63. (original) The transceiver of claim 42, wherein the transceiver employs parallel processing compensation techniques.

64. (original) The transceiver of claim 42, further comprising at least one additional digital signal processor that operates cooperatively with the digital signal processor.

65. (original) The transceiver of claim 42, wherein the transceiver comprises further comprising at least one additional digital signal processor that operates cooperatively with the digital signal processor.

66. (original) The transceiver of claim 42, wherein the transceiver is contained within a first board; and

the integrated circuit is operable to perform serializer/de-serializer data communications with a second board.

67. (original) The transceiver of claim 42, wherein the transceiver is contained within an integrated circuit; and

the integrated circuit is operable to perform serializer/de-serializer data communications with a board.

68. (original) The transceiver of claim 42, wherein the transceiver is contained within a first integrated circuit; and

the integrated circuit is operable to perform serializer/de-serializer data communications with a second integrated circuit.

69. (original) The transceiver of claim 42, wherein the digital signal processor determines the parallel based compensation and the parallel based operation to be performed to ensure the proper characteristic of the digital data; and

the digital signal processor performs the parallel based operation employing digital signal processing to the digital data.

70. (original) The transceiver of claim 42, wherein the digital signal processor is operable to compensate for at least one of near-end crosstalk and far-end crosstalk within the analog serial signal.

71. (original) The transceiver of claim 42, further comprising a crosstalk canceller communicatively coupled to the analog to digital converter; and

wherein the crosstalk canceller is operable to substantially eliminate at least one of near-end crosstalk and far-end crosstalk within the analog serial signal.

72. (original) The transceiver of claim 42, further comprising a decoder that is operable to decode the digital data.

73. (original) The transceiver of claim 72, wherein the decoder comprises at least one of a Viterbi decoder, a convolutional decoder, a block code decoder, and a trellis decoder.

74. (original) The transceiver of claim 73, wherein the Viterbi decoder decodes inter-symbol interference within the modulated serial data.

75. (original) The transceiver of claim 73, wherein the Viterbi decoder comprises a partial response maximum likelihood decoder.

76. (original) The transceiver of claim 42, wherein the transceiver further comprises an analog front-end that comprises a plurality of interleaves; and

the digital signal processor performs adaptive compensation to overcome impairment generated by non-uniformity among the plurality of interleaves.

77. (original) The transceiver of claim 76, wherein the analog front-end comprises a plurality of programmable gain amplifiers; and

the digital signal processor performs adaptive compensation to overcome impairment generated by non-uniformity among the programmable gain amplifiers.

78. (original) The transceiver of claim 76, wherein the analog front-end comprises a plurality of analog to digital converters; and

the digital signal processor performs adaptive compensation to overcome impairment generated by non-uniformity among the plurality of analog to digital converters.

79. (original) The transceiver of claim 42, further comprising wherein the transceiver interfaces to at least one additional device via at least one of a twisted pair cable, a coaxial cable, and a twin-ax cable.

80. (original) A transceiver, comprising:

a receiver comprising a plurality of analog to digital converters and a digital signal processor; and

wherein each analog to digital converter within the plurality of analog to digital converters sequentially samples analog serial signal to generate digital data arranged across a plurality of channels;

each channel of the plurality of channels extends from one analog to digital converter within the plurality of analog to digital converters;

the digital signal processor comprises at least one of a feedback equalizer and a decision feedback equalizer that is operable to adaptively identify error information that is used to determine a parallel based compensation and a parallel based operation to be performed to ensure a proper characteristic of the digital data;

the parallel based operation comprises adjusting an operational parameter of at least one analog to digital converter within the plurality of analog to digital converters; and

the digital signal processor communicates feedback control individually to each analog to digital converter within the plurality of analog to digital converters.

81. (original) The transceiver of claim 80, wherein operational parameter comprises at least one of a sampling rate, an offset, and a phase.

82. (original) The transceiver of claim 80, wherein the adjusting of the operational parameter comprises employing timing recovery.

83. (original) The transceiver of claim 80, wherein the analog serial signal comprises a plurality of band periods; and

the sequential digital sampling of the analog serial signal, as performed by the plurality of analog to digital converters, spans the plurality of band periods.

84. (original) The transceiver of claim 80, wherein the sequential digital sampling of the analog serial signal introduces an error into the digital data.

85. (original) The transceiver of claim 84, wherein the error comprises at least one of an error of gain, an error of phase, and an error of offset.

86. (original) The transceiver of claim 84, wherein the error comprises fixed pattern noise.

87. (original) The transceiver of claim 80, wherein the transceiver receives the analog serial signal via an interconnection; and

the interconnection introduces an error into the analog serial signal.

88. (original) The transceiver of claim 87, wherein the error comprises at least one of an error of inter-symbol interference, attenuation, crosstalk, and noise.

89. (original) The transceiver of claim 80, wherein the analog serial signal is partitioned into a plurality of channels before being fed to the plurality of analog to digital converters.

90. (original) The transceiver of claim 80, further comprising a plurality of programmable gain amplifiers;

wherein the analog serial signal is simultaneously fed to each programmable gain amplifier within the plurality of programmable gain amplifiers; and

each programmable gain amplifier within the plurality of programmable gain amplifiers communicatively couples to one analog to digital converter within the plurality of analog to digital converters.

91. (original) The transceiver of claim 90, wherein the gain of at least one programmable gain amplifier within the plurality of programmable gain amplifiers is adjusted using automatic gain control.

92. (original) The transceiver of claim 80, further comprising an equalizer.

93. (original) The transceiver of claim 92, wherein the equalizer comprises at least one of a feed forward equalizer, a feedback equalizer, and a decision feedback equalizer.

94. (original) The transceiver of claim 80, further comprising a decoder.

95. (original) The transceiver of claim 94, wherein the decoder comprises at least one of a Viterbi decoder, a convolutional decoder, a block code decoder, and a trellis decoder.

96. (original) The transceiver of claim 80, wherein the transceiver is operable to perform data communications at a speed higher than one Giga-bit per second.

97. (original) The transceiver of claim 80, wherein the transceiver employs parallel processing compensation techniques.

98. (original) The transceiver of claim 80, further comprising at least one additional digital signal processor that operates cooperatively with the digital signal processor.

99. (original) The transceiver of claim 80, wherein the transceiver comprises further comprising at least one additional digital signal processor that operates cooperatively with the digital signal processor.

100. (original) The transceiver of claim 80, wherein the transceiver is contained within a first board; and

the integrated circuit is operable to perform serializer/de-serializer data communications with a second board.

101. (original) The transceiver of claim 80, wherein the transceiver is contained within an integrated circuit; and

the integrated circuit is operable to perform serializer/de-serializer data communications with a board.

102. (original) The transceiver of claim 80, wherein the transceiver is contained within a first integrated circuit; and

the integrated circuit is operable to perform serializer/de-serializer data communications with a second integrated circuit.

103. (original) The transceiver of claim 80, wherein the digital signal processor determines the parallel based compensation and the parallel based operation to be performed to ensure the proper characteristic of the digital data; and

the digital signal processor performs the parallel based operation employing digital signal processing to the digital data.

104. (original) The transceiver of claim 80, further comprising a crosstalk canceller communicatively coupled to one analog to digital converter within the plurality of analog to digital converters; and

wherein the crosstalk canceller is operable to substantially eliminate at least one of near-end crosstalk and far-end crosstalk within the analog serial signal.

105. (original) The transceiver of claim 80, further comprising a decoder that is operable to decode the digital data.

106. (original) The transceiver of claim 105, wherein the decoder comprises at least one of a Viterbi decoder, a convolutional decoder, a block code decoder, and a trellis decoder.

107. (original) The transceiver of claim 106, wherein the Viterbi decoder decodes inter-symbol interference within the modulated serial data.

108. (original) The transceiver of claim 106, wherein the Viterbi decoder comprises a partial response maximum likelihood decoder.

109. (original) The transceiver of claim 80, wherein the transceiver further comprises an analog front-end that comprises a plurality of interleaves; and

the digital signal processor performs adaptive compensation to overcome impairment generated by non-uniformity among the plurality of interleaves.

110. (original) The transceiver of claim 109, wherein the analog front-end comprises a plurality of programmable gain amplifiers; and

the digital signal processor performs adaptive compensation to overcome impairment generated by non-uniformity among the programmable gain amplifiers.

111. (original) The transceiver of claim 109, wherein the analog front-end comprises a plurality of analog to digital converters; and

the digital signal processor performs adaptive compensation to overcome impairment generated by non-uniformity among the plurality of analog to digital converters.

112. (original) The transceiver of claim 80, further comprising wherein the transceiver interfaces to at least one additional device via at least one of a twisted pair cable, a coaxial cable, and a twin-ax cable.

113. (original) A method to perform digital signal processing based de-serialization of analog serial signal, the method comprising:

receiving analog serial signal;

digitally sampling the analog serial signal to generate digital data;

analyzing the digital data to determine whether any compensation is required to ensure a proper characteristic of the digital data by employing digital signal processing techniques;

adaptively identifying a compensation operation when it is determined that compensation is required, the compensation operation being selected to ensure the proper characteristic; and

providing compensation control to a device that is operable to perform the compensation operation.

114. (original) The method of claim 113, wherein the compensation operation comprises a parallel based compensation operation.

115. (original) The method of claim 113, wherein the compensation control comprises a parallel based compensation control.

116. (original) The method of claim 113, wherein a digital signal processor analyzes the digital data.

117. (original) The method of claim 113, further comprising identifying an error within the digital data.

118. (original) The method of claim 117, wherein at least one of a feedback equalizer and a decision feedback equalizer identifies the error.

119. (original) The method of claim 113, wherein the digitally sampling of the analog serial signal to generate digital data is performed using a plurality of analog to digital converters.

120. (original) The method of claim 119, wherein the compensation control is provided individually to each analog to digital converter within the plurality of analog to digital converters.

121. (original) The method of claim 113, wherein the device that is operable to perform the compensation operation comprises at least one of an analog to digital converter, a programmable gain amplifier, and a digital signal processor.

122. (original) The method of claim 113, wherein an analog to digital converter performs the digital sampling of the analog serial signal to generate the digital data;

the device that is operable to perform the compensation operation comprises analog circuitry that is situated before the analog to digital converter; and

the analog serial signal passes through both the analog circuitry and the analog to digital converter.

123. (original) The method of claim 113, wherein an analog to digital converter performs the digital sampling of the analog serial signal to generate the digital data;

the device that is operable to perform the compensation operation comprises digital signal processing circuitry that is situated after the analog to digital converter; and

the analog serial signal passes through both the analog to digital converter and the digital signal processing circuitry.

124. (original) The method of claim 113, wherein an analog to digital converter performs the digital sampling of the analog serial signal to generate the digital data;

the device that is operable to perform the compensation operation comprises both analog circuitry that is situated before the analog to digital converter and digital signal processing circuitry that is situated after the analog to digital converter;

the analog serial signal passes through the analog circuitry and the analog to digital converter;

the digital data passes through the digital signal processing circuitry.

125. (original) The method of claim 113, further comprising pre-computing a plurality of possible compensation operation options before identifying the compensation operation; and

selecting at least one compensation operation option from the plurality of possible compensation operation options.

126. (original) The method of claim 113, further comprising partitioning the analog serial signal into a plurality of channels before digitally sampling the analog serial signal to generate digital data.

127. (original) The method of claim 113, further comprising partitioning the analog serial signal into a plurality of channels during the digital sampling of the analog serial signal that generates the digital data.

128. (original) The method of claim 113, further comprising compensating for at least one of near-end crosstalk and far-end crosstalk within the analog serial signal.

129. (original) A method to perform digital signal processing based de-serialization of analog serial signal, the method comprising:

pre-computing a plurality of possible compensation operation options;

receiving analog serial signal;

digitally, sequentially sampling the analog serial signal to generate digital data using a plurality of interleaved analog to digital converters;

analyzing the digital data, using a digital signal processor, to adaptively determine whether any compensation is required to ensure a proper characteristic of the digital data by employing digital signal processing techniques;

selecting a compensation operation when it is determined that compensation is required, the compensation operation being selected to ensure the proper characteristic, the compensation operation being selected from the plurality of possible compensation operation options;

providing compensation control to a device that is operable to perform the compensation operation; and

wherein the compensation, when required, is implemented by adjusting an operational characteristic of at least one analog to digital converter within the plurality of interleaved analog to digital converters.

130. (original) The method of claim 129, wherein the compensation, when required, is implemented by also adjusting an operational characteristic of at least one of an analog circuitry and a digital signal processor.

131. (original) The method of claim 130, wherein the analog circuitry that is situated before the plurality of interleaved analog to digital converters.

132. (original) The method of claim 130, wherein digital signal processor is situated after the plurality of interleaved analog to digital converters.

133. (original) The method of claim 129, further comprising compensating for at least one of near-end crosstalk and far-end crosstalk within the analog serial signal.

134. (original) A digital signal processing based serializer/de-serializer, comprising:

a receiver that includes an analog to digital converter and a digital signal processor that is operably coupled to an output of the analog to digital converter;

wherein the analog to digital converter samples modulated serial data to generate digital samples of the modulated serial data;

the modulated serial data is provided to the receiver by a serializer/de-serializer transmitter across at least one of a trace on a printed circuit board and a backplane; and

the digital signal processor demodulates the digital samples to extract the digital data contained therein.

135. (original) The digital signal processing based serializer/de-serializer of claim 134, wherein the digital signal processor adaptively determines compensation operations to be performed by the receiver on the digital samples of the modulated serial data so that the digital samples of the modulated serial data may be properly characterized to extract digital data contained therein.

136. (original) The digital signal processing based serializer/de-serializer of claim 134, wherein the digital signal processing based serializer/de-serializer interfaces a first printed circuit board to a second printed circuit board.

137. (original) The digital signal processing based serializer/de-serializer of claim 134, wherein the digital signal processing based serializer/de-serializer interfaces a first integrated circuit to a second integrated circuit.

138. (original) The digital signal processing based serializer/de-serializer of claim 137, wherein the plurality of integrated circuits are situated on a printed circuit board.

139. (original) The digital signal processing based serializer/de-serializer of claim 134, wherein at least one of the analog serial data and the digital data comprises fixed pattern noise.

140. (original) The digital signal processing based serializer/de-serializer of claim 139, wherein the digital signal processor determines compensation to be performed to substantially eliminate the fixed pattern noise.

141. (original) The digital signal processing based serializer/de-serializer of claim 139, wherein the fixed pattern noise is introduced during the digital sampling of the analog serial data by the analog to digital converter to generate the digital data.

142. (original) The digital signal processing based serializer/de-serializer of claim 134, wherein the digital signal processor determines a compensation operation to be performed on the analog serial data.

143. (original) The digital signal processing based serializer/de-serializer of claim 142, further comprising a programmable gain amplifier, communicatively coupled to the analog to digital converter; and

wherein the compensation operation comprises adjusting the gain of the programmable gain amplifier.

144. (original) The digital signal processing based serializer/de-serializer of claim 143, further comprising an automatic gain control circuitry; and

wherein the automatic gain control circuitry adjusts the gain of the programmable gain amplifier.

145. (original) The digital signal processing based serializer/de-serializer of claim 134, wherein the digital signal processor determines a compensation operation to be performed on the digital data.

146. (original) The digital signal processing based serializer/de-serializer of claim 134, wherein the digital signal processing based serializer/de-serializer is implemented in a data communications application.

147. (original) The digital signal processing based serializer/de-serializer of claim 134, further comprising a memory that comprises a plurality of compensation options;

wherein the digital signal processor selects at least one compensation option from the plurality of compensation options to ensure the proper characteristic of the digital data.

148. (original) The digital signal processing based serializer/de-serializer of claim 134, wherein the proper characteristic of the digital data comprises at least one of a gain, a phase, and an offset.

149. (original) The digital signal processing based serializer/de-serializer of claim 134, further comprising a transmitter and an interconnection; and

wherein the interconnection communicatively couples the transmitter and the receiver;

the transmitter transmits the serial data to the receiver via the interconnection;

the interconnection comprises a response that introduces an error into the serial data;

the digital signal processor determines the error introduced into the serial data by the response of the interconnection.

150. (original) The digital signal processing based serializer/de-serializer of claim 134, wherein the proper characteristic of the digital data comprises at least one of a gain, a phase, and an offset; and

the digital signal processor determines at least one of an error in gain, an error in phase, and an error in offset that is introduced during the digital sampling of the incoming, serial data signal by the analog to digital converter.

151. (original) The digital signal processing based serializer/de-serializer of claim 134, wherein the compensation determined by the digital signal processor comprises a compensation operation that comprises adjusting an operational parameter of the analog to digital converter.

152. (original) The digital signal processing based serializer/de-serializer of claim 134, further comprising an analog circuitry located before and communicatively coupled to the analog to digital converter; and

wherein the compensation determined by the digital signal processor comprises a compensation operation that comprises adjusting an operational parameter of the analog circuitry.

153. (original) The digital signal processing based serializer/de-serializer of claim 134, wherein the analog to digital converter comprises a plurality of analog to digital converters; and

each analog to digital converter within the plurality of analog to digital converters performs digital sampling of the incoming, serial data signal.

154. (original) The digital signal processing based serializer/de-serializer of claim 153, each analog to digital converter within the plurality of analog to digital converters performs digital sampling of a clock cycle of the analog serial data at a different time.

155. (original) The digital signal processing based serializer/de-serializer of claim 154, wherein the compensation determined by the digital signal processor comprises a compensation operation that comprises adjusting a first operational parameter of a first analog to digital converter within the plurality of analog to digital converters and a second operational parameter of a second analog to digital converter within the plurality of analog to digital converters.

156. (original) The digital signal processing based serializer/de-serializer of claim 155, wherein the first operational parameter and the second operational parameter comprise a common operational parameter.

157. (original) The digital signal processing based serializer/de-serializer of claim 155, wherein at least one of the first operational parameter and the second operational parameter comprises at least one of a gain, a phase, and an offset.

158. (original) The digital signal processing based serializer/de-serializer of claim 134, wherein the analog to digital converter comprises a plurality of analog to digital converters;

the analog serial data is partitioned into a plurality of channels; and

each channel of the plurality of channels communicatively couples to one analog to analog to digital converter within the plurality of analog to digital converters.

159. (original) The digital signal processing based serializer/de-serializer of claim 158, further comprising a plurality of programmable gain amplifiers;

the analog serial data is simultaneously fed to each programmable gain amplifier within the plurality of programmable gain amplifiers;

the outputs of the plurality of programmable gain amplifiers form the plurality of channels.

160. (original) The digital signal processing based serializer/de-serializer of claim 134, wherein the analog to digital converter comprises a plurality of analog to digital converters;

the analog serial data is simultaneously fed to each analog to digital converter within the plurality of analog to digital converters.

161. (original) The digital signal processing based serializer/de-serializer of claim 134, further comprising a precursor filter and an equalizer;

wherein the precursor filter is communicatively coupled to the analog to digital converter; and

the equalizer is communicatively coupled to the analog to digital converter.

162. (original) The digital signal processing based serializer/de-serializer of claim 161, wherein the equalizer comprises at least one of a feed forward equalizer, a feedback equalizer, and a decision feedback equalizer.

163. (original) The digital signal processing based serializer/de-serializer of claim 134, further comprising a decoder that is operable to decode the digital samples of the modulated serial data.

164. (original) The digital signal processing based serializer/de-serializer of claim 163, wherein the decoder comprises at least one of a Viterbi decoder, a convolutional decoder, a block code decoder, and a trellis decoder.

165. (original) The digital signal processing based serializer/de-serializer of claim 164, wherein the Viterbi decoder decodes inter-symbol interference within the modulated serial data.

166. (original) The digital signal processing based serializer/de-serializer of claim 164, wherein the Viterbi decoder comprises a partial response maximum likelihood decoder.

167. (original) The digital signal processing based serializer/de-serializer of claim 134, wherein the digital signal processing based serializer/de-serializer is operable to perform data communications at a speed higher than one Giga-bit per second.

168. (original) The digital signal processing based serializer/de-serializer of claim 134, wherein the digital signal processing based serializer/de-serializer employs parallel processing compensation techniques.

169. (original) The digital signal processing based serializer/de-serializer of claim 134, further comprising at least one additional digital signal processor that operates cooperatively with the digital signal processor.

170. (original) The digital signal processing based serializer/de-serializer of claim 134, wherein the digital signal processor is operable to perform digital signal processing on the digital data to ensure the proper characteristic of the digital data.

171. (original) The digital signal processing based serializer/de-serializer of claim 134, further comprising a crosstalk canceller communicatively coupled to the analog to digital converter; and

wherein the crosstalk canceller is operable to substantially eliminate at least one of near-end crosstalk and far-end crosstalk within the modulated serial data.

172. (original) The digital signal processing based serializer/de-serializer of claim 134, wherein the receiver further comprises an analog front-end that comprises a plurality of interleaves; and

the digital signal processor performs adaptive compensation to overcome impairment generated by non-uniformity among the plurality of interleaves.

173. (original) The digital signal processing based serializer/de-serializer of claim 172, wherein the analog front-end comprises a plurality of programmable gain amplifiers; and

the digital signal processor performs adaptive compensation to overcome impairment generated by non-uniformity among the programmable gain amplifiers.

174. (original) The digital signal processing based serializer/de-serializer of claim 172, wherein the analog front-end comprises a plurality of analog to digital converters; and

the digital signal processor performs adaptive compensation to overcome impairment generated by non-uniformity among the plurality of analog to digital converters.

175. (original) A transceiver, comprising:

a serializer/de-serializer receiver, that receives modulated serial data from a serializer/de-serializer transmitter, that includes a plurality of interleaved analog to digital converters and a digital signal processor, the digital signal processor being communicatively coupled to an output of the plurality of interleaved analog to digital converters;

the plurality of interleaved analog to digital converters operate cooperatively to sample the modulated serial data to generate digital samples of the modulated serial data; and

the digital signal processor demodulates the digital samples to extract the digital data contained therein.

176. (original) A transceiver, comprising:

a serializer/de-serializer receiver, that receives modulated serial data from a serializer/de-serializer transmitter, that includes a plurality of interleaved analog to digital converters and a digital signal processor, the digital signal processor being communicatively coupled to an output of the plurality of interleaved analog to digital converters;

the plurality of interleaved analog to digital converters operate cooperatively to sample the modulated serial data to generate digital samples of the modulated serial data;

the digital signal processor employs parallel processing techniques to compensate for non-uniformity among interleaves of the plurality of interleaved analog to digital converters; and

the digital signal processor demodulates the digital samples using parallel processing techniques to extract the digital data contained therein.

177. (original) A transceiver, comprising:

a serializer/de-serializer receiver that includes a plurality of interleaved analog to digital converters and a digital signal processor, the digital signal processor being communicatively coupled to an output of the plurality of interleaved analog to digital converters;

the plurality of interleaved analog to digital converters operate cooperatively to sample modulated serial data to generate digital samples of the modulated serial data;

the digital signal processor employs parallel processing techniques to compensate for non-uniformity among interleaves of the plurality of interleaved analog to digital converters;

the modulated serial data is provided to the serializer/de-serializer receiver by a serializer/de-serializer transmitter across at least one of a trace on a printed circuit board and a backplane; and

the digital signal processor demodulates the digital samples using parallel processing techniques to extract the digital data contained therein.

178. (original) A transceiver, comprising:

a serializer/de-serializer receiver that includes a plurality of interleaved analog to digital converters and a digital signal processor, the digital signal processor being communicatively coupled to an output of the plurality of interleaved analog to digital converters;

the plurality of interleaved analog to digital converters operate cooperatively to sample modulated serial data to generate digital samples of the modulated serial data;

the modulated serial data is provided to the serializer/de-serializer receiver by a serializer/de-serializer transmitter across at least one of a trace on a printed circuit board and a backplane; and

the digital signal processor demodulates the digital samples to extract the digital data contained therein.

179. (original) A transceiver, comprising:

a serializer/de-serializer receiver, that receives the modulated serial data from a serializer/de-serializer transmitter, that includes an analog to digital converter and a

digital signal processor, the digital signal processor being communicatively coupled to an output of the analog to digital converter;

the analog to digital converter samples modulated serial data to generate digital samples of the modulated serial data; and

the digital signal processor demodulates the digital samples using parallel processing techniques to extract the digital data contained therein.

180. (original) A transceiver, comprising:

a serializer/de-serializer receiver that includes an analog to digital converter and a digital signal processor, the digital signal processor being communicatively coupled to an output of the analog to digital converter;

the analog to digital converter samples modulated serial data to generate digital samples of the modulated serial data;

the modulated serial data is provided to the serializer/de-serializer receiver by a serializer/de-serializer transmitter across at least one of a trace on a printed circuit board and a backplane; and

the digital signal processor demodulates the digital samples using parallel processing techniques to extract the digital data contained therein.

181. (original) A transceiver, comprising:

a serializer/de-serializer receiver, that receives modulated serial data from a serializer/de-serializer transmitter, that includes a plurality of interleaved analog to digital converters and a digital signal processor, the digital signal processor being communicatively coupled to an output of the plurality of interleaved analog to digital converters;

the plurality of interleaved analog to digital converters operate cooperatively to sample the modulated serial data to generate digital samples of the modulated serial data; and

the digital signal processor demodulates the digital samples using parallel processing techniques to extract the digital data contained therein.

182. (original) A transceiver, comprising:

a serializer/de-serializer receiver the digital signal processor being communicatively coupled to an output of the plurality of interleaved analog to digital converters;

the plurality of interleaved analog to digital converters operate cooperatively to sample modulated serial data to generate digital samples of the modulated serial data;

the modulated serial data is provided to the serializer/de-serializer receiver by a serializer/de-serializer transmitter across at least one of a trace on a printed circuit board and a backplane; and

the digital signal processor demodulates the digital samples using parallel processing techniques to extract the digital data contained therein.

183. (original) A transceiver, comprising:

a serializer/de-serializer receiver, that receives modulated serial data from a serializer/de-serializer transmitter, that includes a plurality of interleaved analog to digital converters and a digital signal processor, the digital signal processor being communicatively coupled to an output of the plurality of interleaved analog to digital converters;

the plurality of interleaved analog to digital converters operate cooperatively to sample the modulated serial data to generate digital samples of the modulated serial data;

the digital signal processor compensates for non-uniformity among interleaves of the plurality of interleaved analog to digital converters; and

the digital signal processor demodulates the digital samples to extract the digital data contained therein.

184. (original) A transceiver, comprising:

a serializer/de-serializer receiver that includes a plurality of interleaved analog to digital converters and a digital signal processor, the digital signal processor being communicatively coupled to an output of the plurality of interleaved analog to digital converters;

the plurality of interleaved analog to digital converters operate cooperatively to sample modulated serial data to generate digital samples of the modulated serial data;

the digital signal processor compensates for non-uniformity among interleaves of the plurality of interleaved analog to digital converters;

the modulated serial data is provided to the serializer/de-serializer receiver by a serializer/de-serializer transmitter across at least one of a trace on a printed circuit board and a backplane; and

the digital signal processor demodulates the digital samples to extract the digital data contained therein.